Claims

We claim:

1. A memory interface system, comprising:

at least one channel line that couples a memory to a memory controller, the at least one channel line being responsive to a terminal voltage that is independent of a memory supply voltage and a memory controller supply voltage.

2. The memory interface system of Claim 1, wherein the memory comprises a first transmitter and a first receiver, the memory controller comprises a second transmitter and a second receiver, and the at least one channel line comprises a first channel line that couples the first transmitter to the second receiver and a second channel line that couples the second transmitter to the first receiver.

3. The memory interface system of Claim 2, wherein the first and second receivers are powered by the memory supply voltage and the memory controller supply voltage, respectively.

4. The memory interface system of Claim 3, wherein the first and second transmitters are operable independent from the memory supply voltage and the memory controller supply voltage, respectively.

5. The memory interface system of Claim 2, further comprising:

a first level shifter circuit that couples the second channel line to the first receiver; and

a second level shifter circuit that couples the first channel line to the second receiver.

6. The memory interface system of Claim 2, wherein the first and second transmitters respectively comprise first and second open-drain MOS transistors.

7. The memory interface system of Claim 2, wherein the first and second receivers respectively comprise first and second differential amplifier circuits.

8. The memory interface system of Claim 7, wherein the first differential amplifier circuit is responsive to a first reference voltage and a data signal carried on the second channel line, and wherein the second differential amplifier circuit is responsive to a second reference voltage and a data signal carried on the first channel line.

9. The memory interface system of Claim 7, further comprising:

a first level shifter circuit that couples the second channel line to the first differential amplifier circuit; and

a second level shifter circuit that couples the first channel line to the second differential amplifier circuit.

10. The memory interface system of Claim 1, wherein a magnitude of the terminal voltage is greater than magnitudes of the memory supply voltage and the controller supply voltage, respectively.

11. A data processing system, comprising:

a memory that is responsive to a memory supply voltage;

a memory controller that is responsive to a memory controller supply voltage; and

at least one channel line that couples the memory to the memory controller, the at least one channel line being responsive to a terminal voltage that is independent of the memory supply voltage and the memory controller supply voltage.

12. The data processing system of Claim 11, wherein the memory comprises a first transmitter and a first receiver, the memory controller comprises a second transmitter and a second receiver, and the at least one channel line comprises a first channel line that couples the first transmitter to the second receiver and a second channel line that couples the second transmitter to the first receiver.

13. The data processing system of Claim 12, wherein the first and second receivers are powered by the memory supply voltage and the memory controller supply voltage, respectively.

14. The data processing system of Claim 13, wherein the first and second transmitters are operable independent from the memory supply voltage and the memory controller supply voltage, respectively.

15. The data processing system of Claim 12, further comprising:

a first level shifter circuit that couples the second channel line to the first receiver; and

a second level shifter circuit that couples the first channel line to the second receiver.

16. The data processing system of Claim 12, wherein the first and second transmitters respectively comprise first and second open-drain MOS transistors.

17. The data processing system of Claim 12, wherein the first and second receivers respectively comprise first and second differential amplifier circuits.

18. The data processing system of Claim 17, wherein the first differential amplifier circuit is responsive to a first reference voltage and a data signal carried on the second channel line, and wherein the second differential amplifier circuit is responsive to a second reference voltage and a data signal carried on the first channel line.

19. The data processing system of Claim 17, further comprising:

a first level shifter circuit that couples the second channel line to the first differential amplifier circuit; and

a second level shifter circuit that couples the first channel line to the second differential amplifier circuit.

20. The data processing system of Claim 11, wherein a magnitude of the terminal voltage is greater than magnitudes of the memory supply voltage and the controller supply voltage, respectively.

21. A memory interface system, comprising:

a channel line that couples a memory to a memory controller;

a transmitter that is configured to transmit a data signal on the channel line; and

a receiver that is configured to compare the data signal with a reference voltage to generate a received signal.

22. The memory interface system of Claim 21, further comprising:

a level shifter circuit that couples the channel line to the receiver.

23. The memory interface system of Claim 21, wherein the transmitter comprises an open-drain MOS transistor.

24. The memory interface system of Claim 21, wherein the receiver comprises a differential amplifier circuit.